700V, 6A, 1251mΩ N-channel Power Planar MOSFET

JMPK6N70BJ

Features

- Excellent R_{DS(ON)} and Low Gate Charge
- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

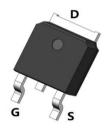
Applications

- SMPS with PFC and Flyback
- Silver ATX,adapter,TV,lighting,Telecom

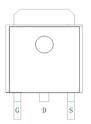
Product Summary

Parameters	Value	Unit
V_{DSS}	700	V
$V_{GS(th)_Typ}$	3.0	V
$I_{D}(@V_{GS}=10V)$	6	Α
$R_{DS(ON)_Typ}(@V_{GS}=10V$	1251	mΩ

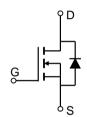




TO-252-3L Top View



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMPK6N70BJ	JMPK6N70BJ	3	Tape&Reel	TO-252-3L	2500	25000

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit	
V_{DS}	Drain-to-Source Voltage		700	V	
V_{GS}	Gate-to-Source Voltage		±30	V	
I_	Continuous Drain Current	$T_C = 25^{\circ}C$	6	А	
I _D		$T_C = 100$ °C	4		
I _{DM}	Pulsed Drain Current (1)		Refer to Fig.4	Α	
E _{AS}	Single Pulsed Avalanche Energy (2)		157	mJ	
P _D		$T_C = 25^{\circ}C$	50	W	
		$T_{\rm C} = 100^{\circ}{\rm C}$	20]	
T_{J}, T_{STG}	Junction & Storage Temperature Range		-55 to 150	°C	

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	61	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	C/ VV



Electrical Characteristics (T_J = 25°C unless otherwise specified)

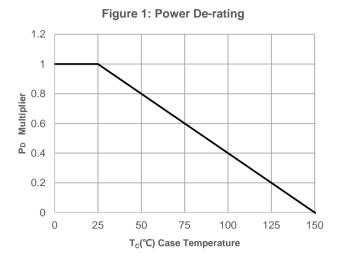
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Cha	racteristics					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	700	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 700V, V_{GS} = 0V$	-	-	1.0	μА
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 30V$	-	-	±100	nA
On Cha	racteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.1	3.0	3.9	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10V, I_{D} = 3A$	-	1251	1627	mΩ
Dynami	c Characteristics					
R_{g}	Gate Resistance	f = 1MHz	1	2.3	-	Ω
C_{iss}	Input Capacitance	., ., ., ., ., ., ., ., ., ., ., ., ., .	-	1144	-	pF
C_{oss}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 350V,$ f = 1MHz	-	30	-	pF
C_{rss}	Reverse Transfer Capacitance	1 – 111112	-	7.4	-	pF
Q_g	Total Gate Charge		-	24	-	nC
Q_gs	Gate Source Charge	$V_{GS} = 0 \text{ to } 10V$ $V_{DS} = 350V, I_{D} = 3A$	-	6.0	-	nC
Q_{gd}	Gate Drain("Miller") Charge	V _{DS} = 000 V, 1 _D = 070	1	7.0	-	nC
Switchi	ng Characteristics					
t _{d(on)}	Turn-On DelayTime		_	12	-	ns
` ′	Turn-On Rise Time	$V_{GS} = 10V, V_{DD} = 350V$	-	16	-	ns
t _{d(off)}	Turn-Off DelayTime	$I_D = 3A$, $R_{GEN} = 6\Omega$	-	32	-	ns
t _f	Turn-Off Fall Time		-	23	-	ns
Body D i	iode Characteristics					
I_S	Maximum Continuous Body Diode Forward Current		-	-	6	Α
I _{SM}	Maximum Pulsed Body Diode Forward Current		-	-	24	Α
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0V$, $I_S = 3A$	-		1.2	V
trr	Body Diode Reverse Recovery Time	1 - 24 di/d+ 4004/:	-	261	-	ns
Qrr	Body Diode Reverse Recovery Charge	$I_F = 3A$, di/dt = 100A/us	-	1998	-	nC

Notes:

- 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
- $2.~E_{AS}~condition:~Starting~T_J=25C,~V_{DD}=50V,~V_{GS}=10V,~R_G=25ohm,~L=10mH,~I_{AS}=5.6A,~V_{DD}=0V~during~time~in~avalanche.$
- $3.~R_{BJA}$ is measured with the device mounted on FR-4 substrate PC board, 20z copper, with minimum recommended pad layout.
- 4. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%.



Typical Performance Characteristics



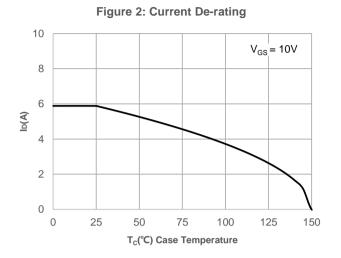
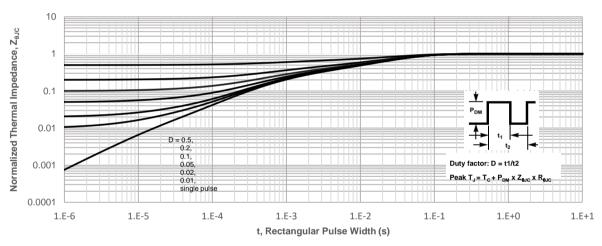
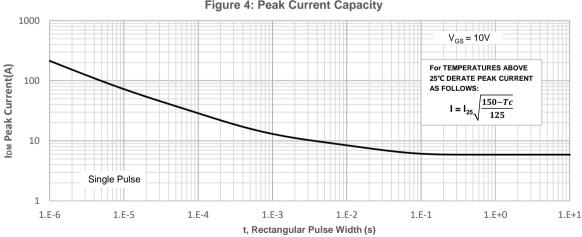


Figure 3: Normalized Maximum Transient Thermal Impedance







Typical Performance Characteristics

Figure 5: Output Characteristics

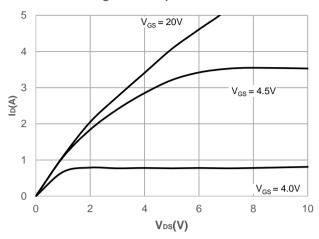


Figure 6: Typical Transfer Characteristics

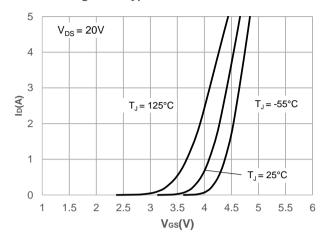


Figure 7: On-resistance vs. Drain Current

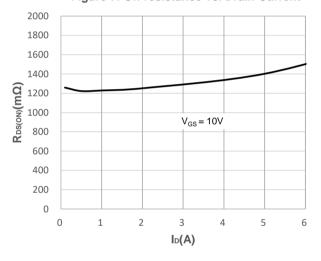


Figure 8: Body Diode Characteristics

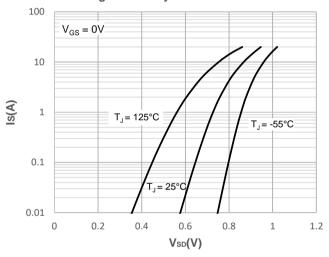


Figure 9: Gate Charge Characteristics

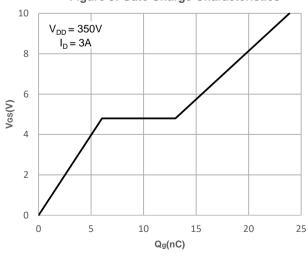
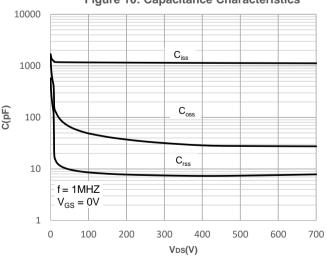


Figure 10: Capacitance Characteristics





Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs.
Junction Temperature

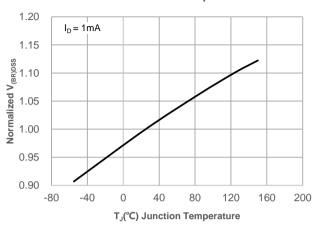


Figure 13: Normalized Threshold Voltage vs.
Junction Temperature

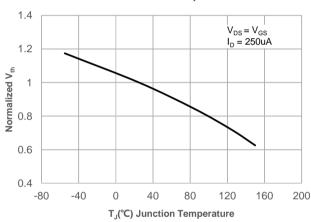


Figure 15: Maximum Safe Operating Area

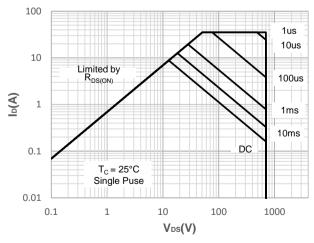
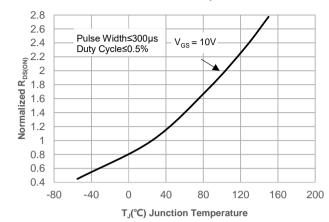
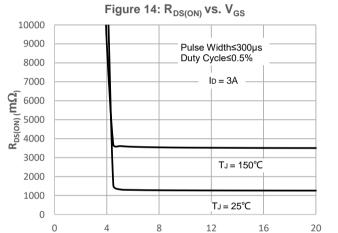


Figure 12: Normalized on Resistance vs.
Junction Temperature





V_{GS}(V)



Test Circuit

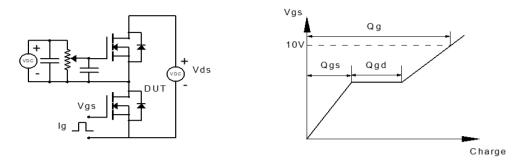


Figure 1: Gate Charge Test Circuit & Waveform

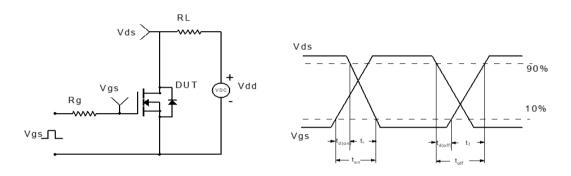


Figure 2: Resistive Switching Test Circuit & Waveform

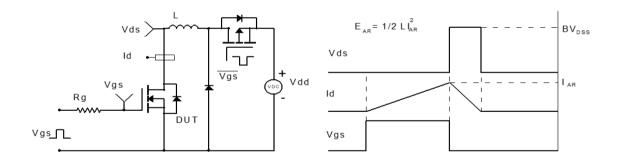


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

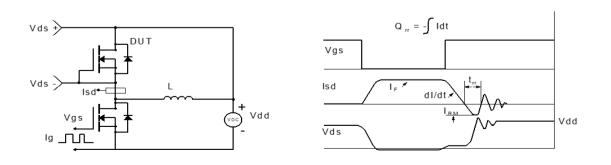
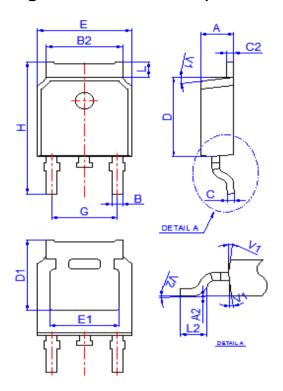


Figure 4: Diode Recovery Test Circuit & Waveform

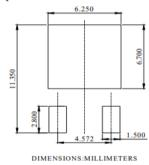


Package Mechanical Data(TO-252-3L)



			Dime	ensions		
Ref.	M il lim eters			Inches		
	M in.	Тур.	Max.	Min.	Тур.	Max.
Α	2.10		2.50	0.083		0.098
A2	0		0.15	0		0.006
В	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
С	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1		5.30REF		0.209RE F		
E	6.40		6.80	0.252		0.268
E 1	4.63			0.182		
G	4.47		4.67	0.176		0.184
Н	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Recommended Soldering Footprint



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